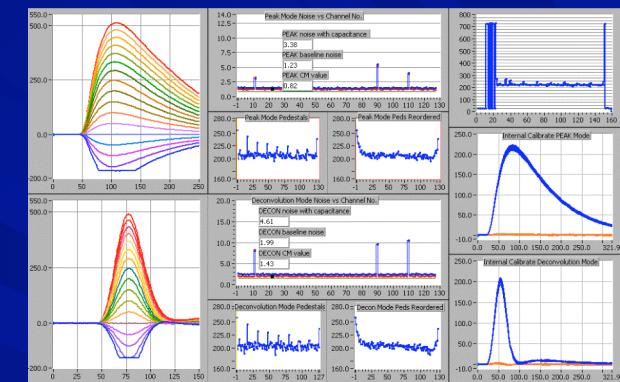


# Electronics

dapnia  
—  
cea  
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saclay



By P. Le Dû

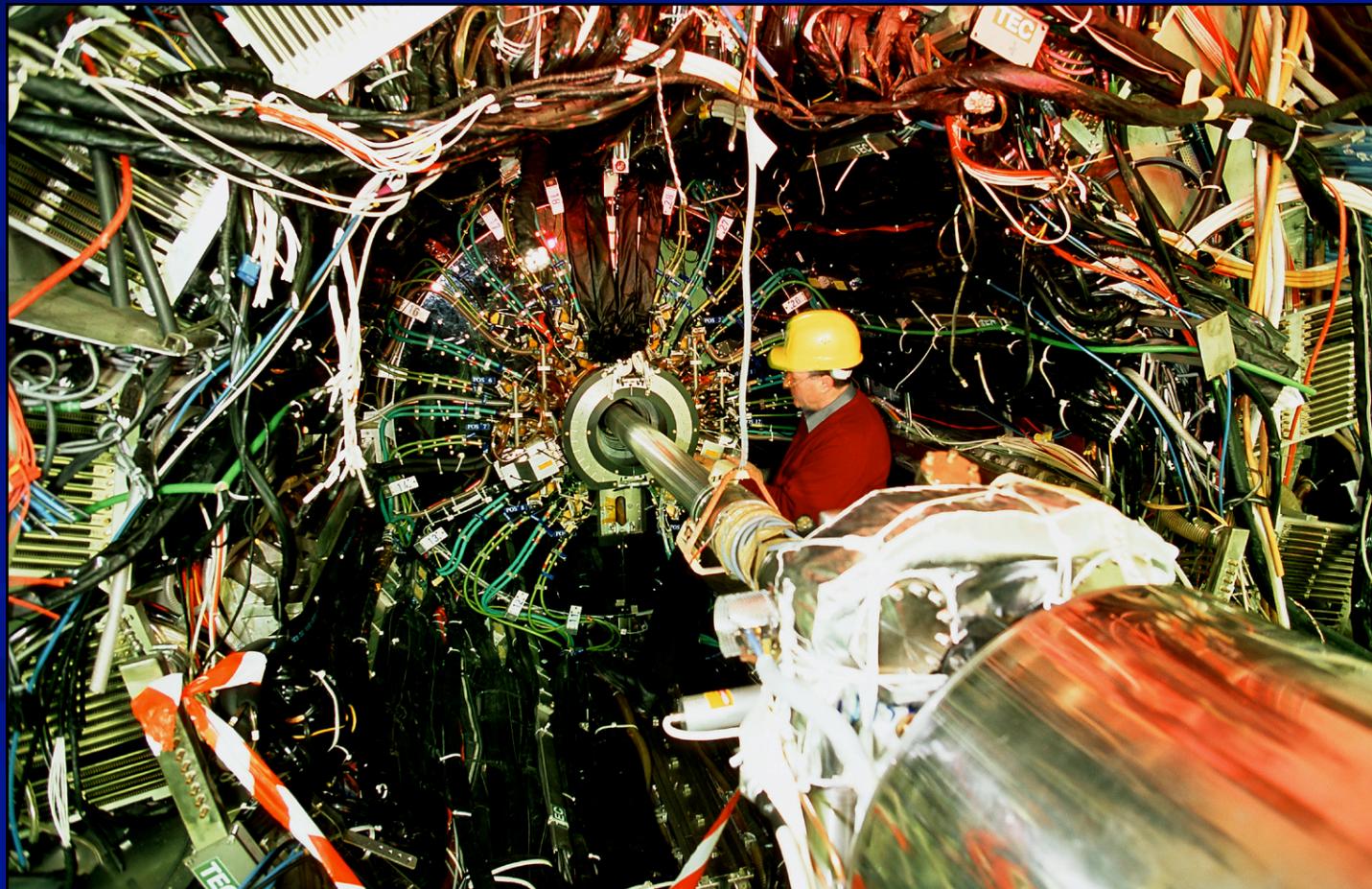
[patrick.le-du@cea.fr](mailto:patrick.le-du@cea.fr)

Thanks to Ch. Delataille (LAL) and J.F. Genat (LPNHE)

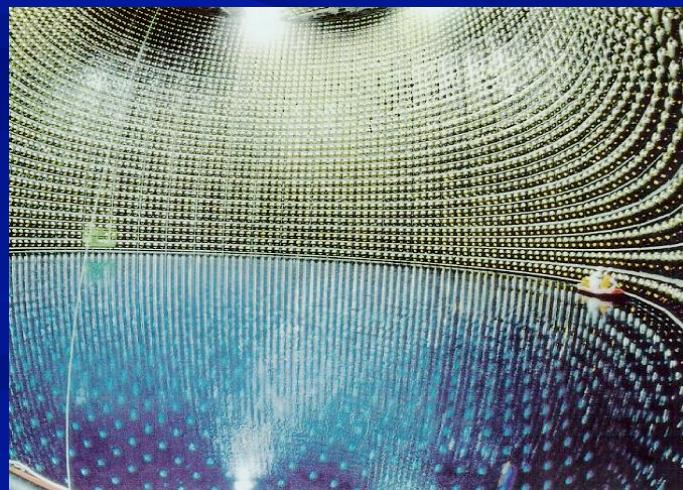
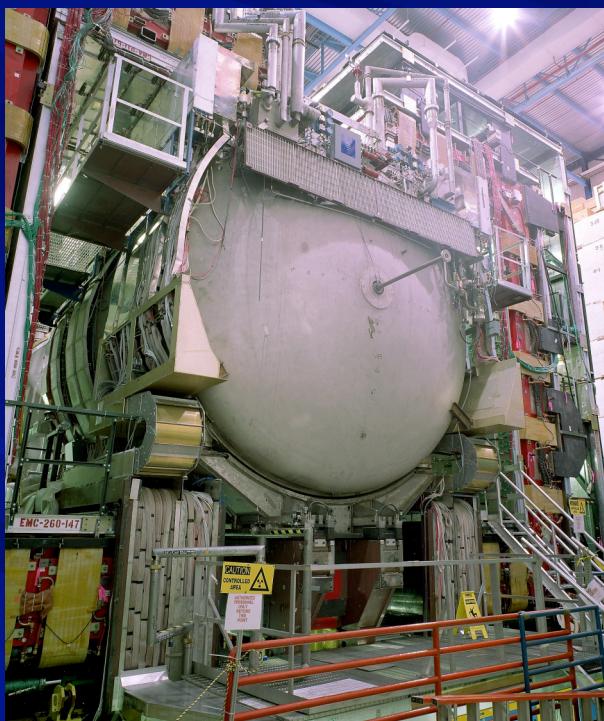
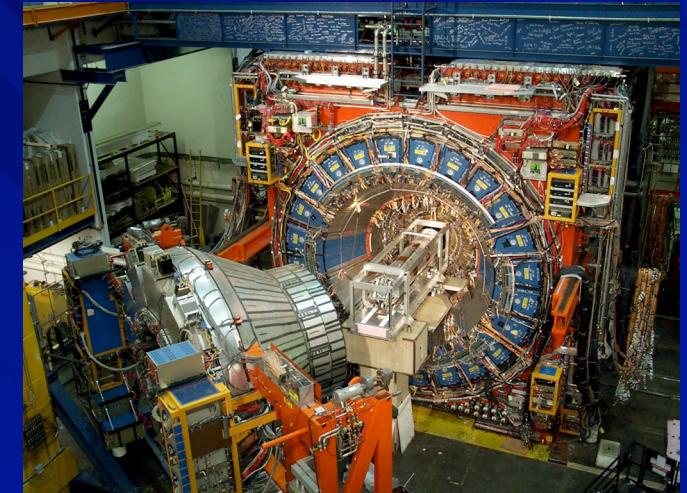
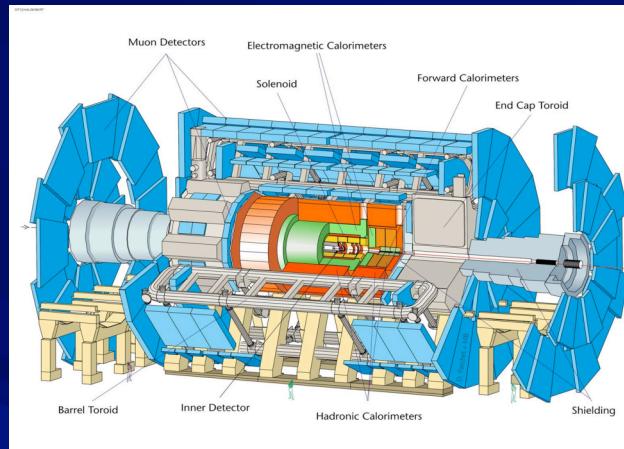
# Electronics in experiments

## ■ A lot of electronics in the experiments...

- Readout electronics : amplification, filtering... : **Analog electronics (A,V,C)**
- Processing & Trigger electronics : **Digital electronics (bits)**
- The performance of electronics often impacts on the detectors

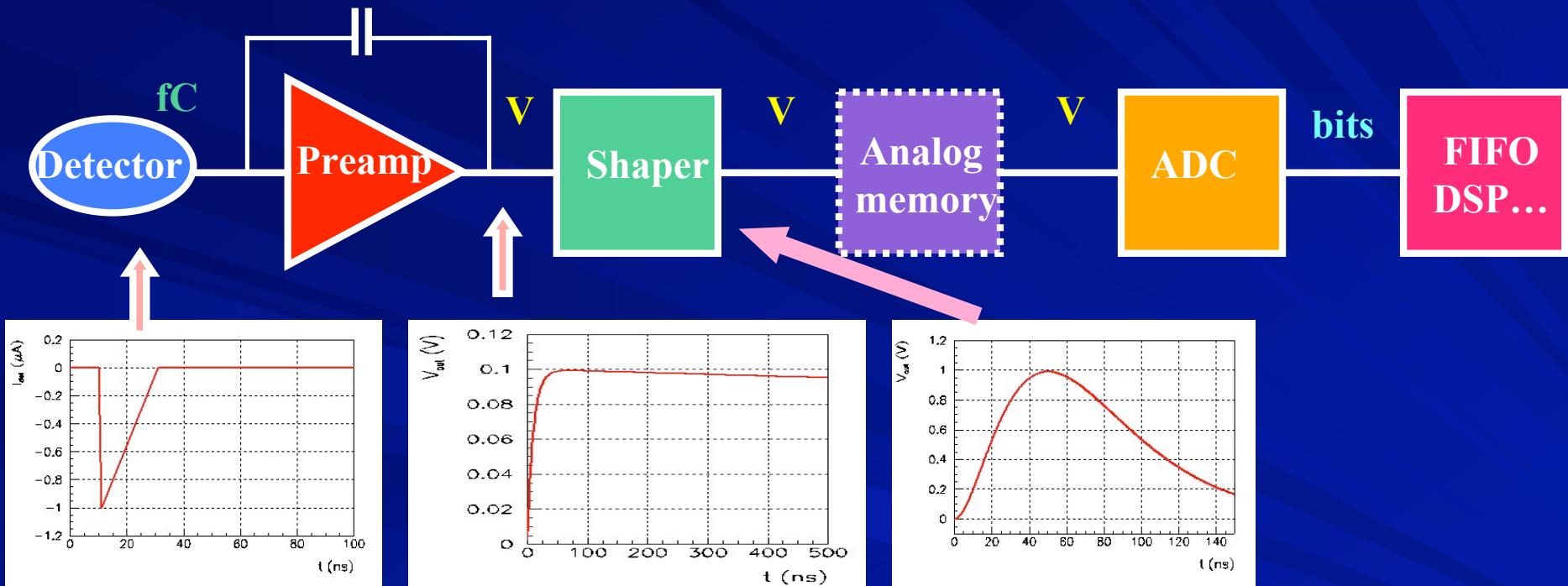


# Many different detectors

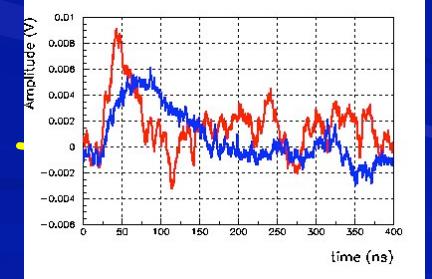


# Overview of readout electronics

- Most front-ends follow a similar architecture



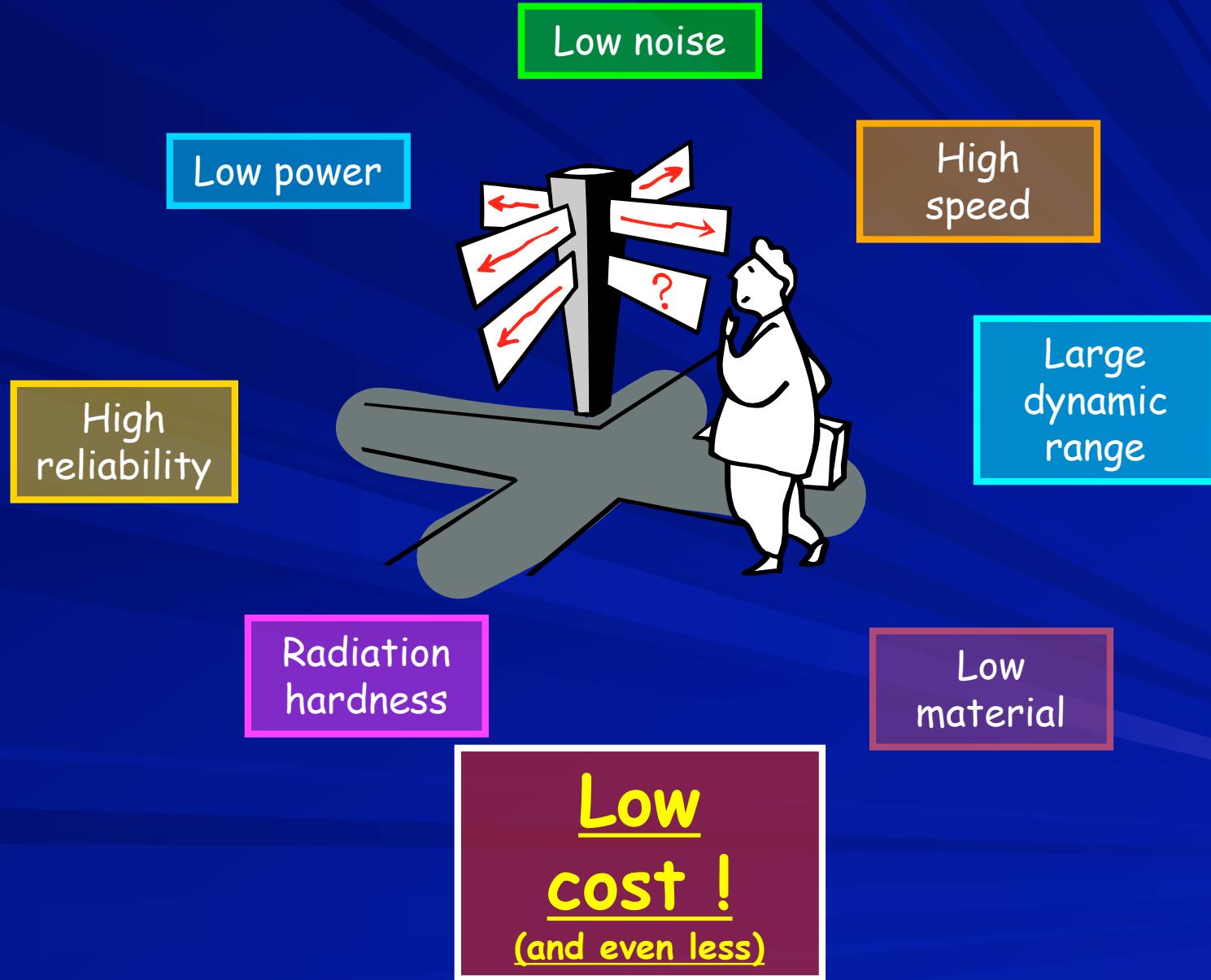
- Very small signals ( $fC$ ) -> need amplification
- Measurement of amplitude and/or time (ADCs, discriminators)
- Several thousands to millions of channels



Noises

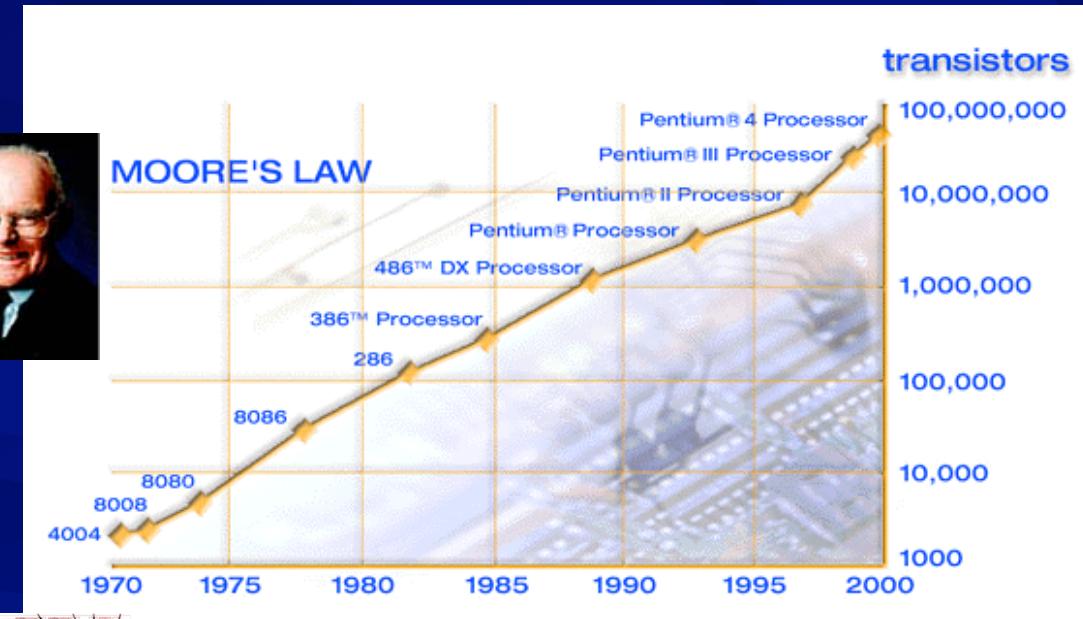
4

# Readout electronics : requirements

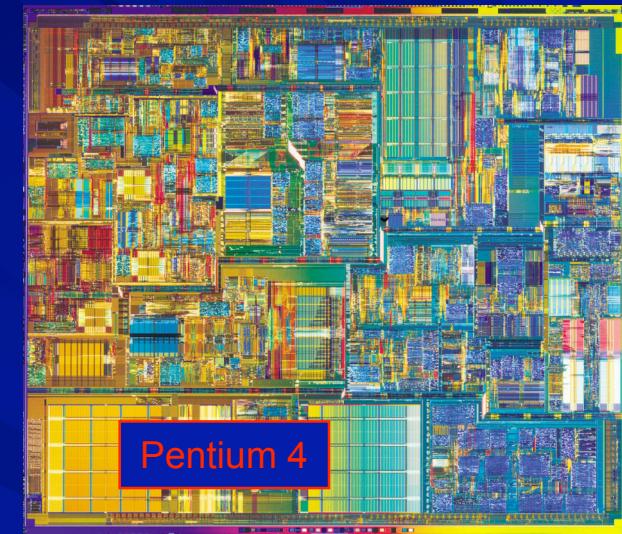


# Evolution of CMOS technologies

■ Moore's law : doubling every 2 years

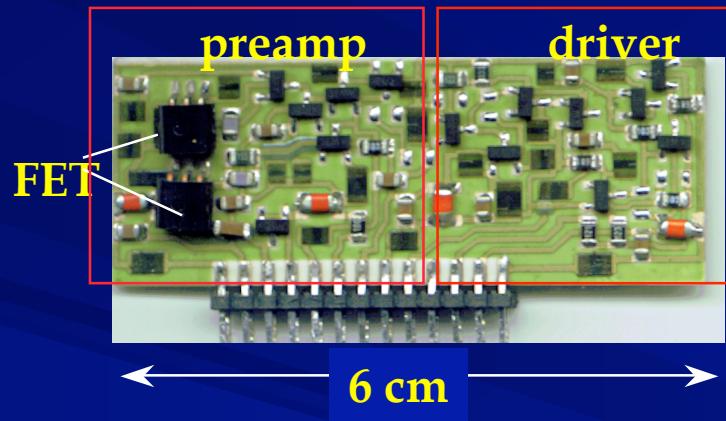


Micropuceur	4004	8086	i386	Pentium	Pentium 4
Année	1971	1978	1985	1993	2000
Nb. Bits	4	16	32	64	64
Horloge (Hz)	108k	10M	33M	66M	1.5G
Mémoire adressable (bytes)	640	1M	16M	4G	64G
Technologie ( $\mu\text{m}$ )	10	3	1	0.8	0.18
Nb transistors	2300	29000	275000	3.1M	42M
Tension alim (V)	12	5	5	5/3.3	1.3 interne

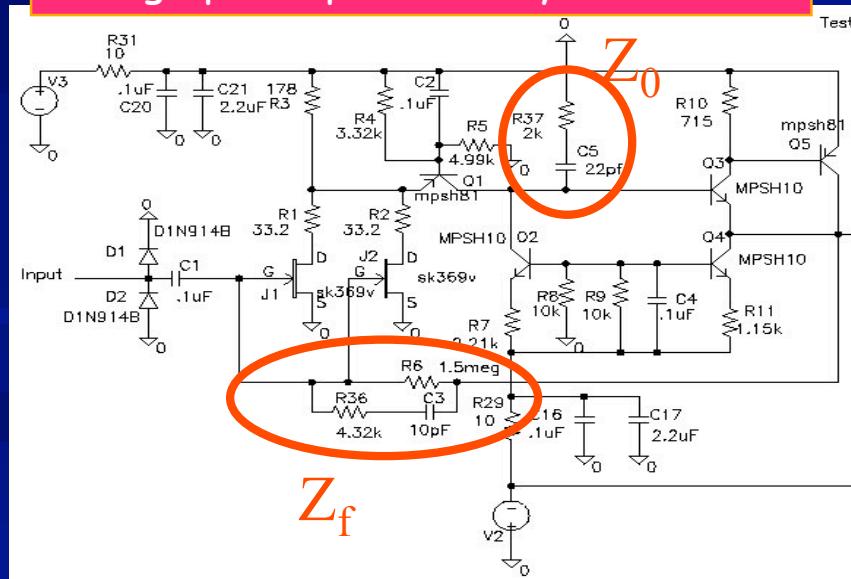


# (R)evolution of analog electronics (1)

## The revolution of microelectronics

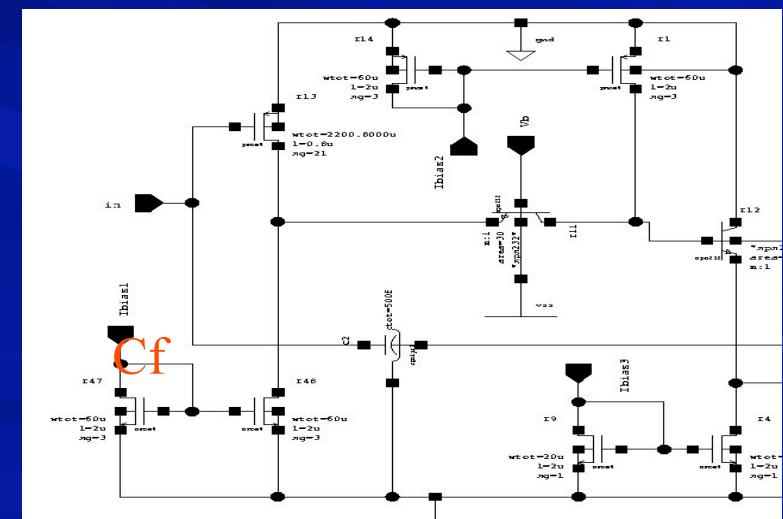
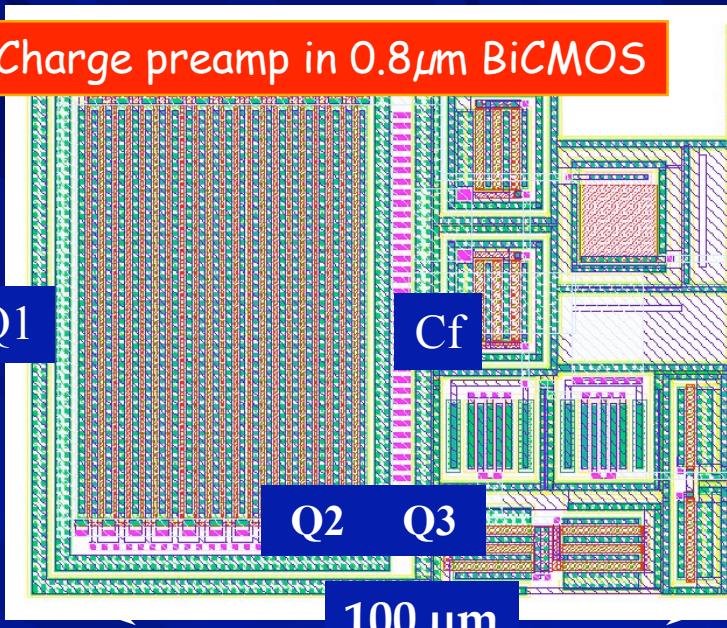


Charge preamp in SMC hybrid techno



1980

Charge preamp in 0.8 μm BiCMOS



ToDay

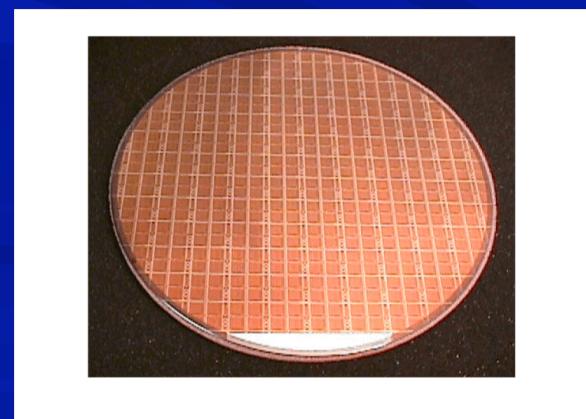
# (R)evolution of analog electronics (2)

## ■ ASICs : Application Specific Integrated Circuits

- Access to foundries through **multiproject (MPW) runs**
- Affordable : 600 €/mm<sup>2</sup>
- Full custom layout, at transistor level
- Mostly **CMOS, BiCMOS technologies**

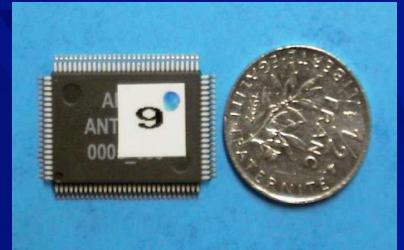
## ■ Widespread in HEP

- High level of integration in minimal area, limited mostly by power dissipation and EMC/EMI
- Improved performance : reduction of parasitics
- Improved reliability (less connections)
- But longer development time



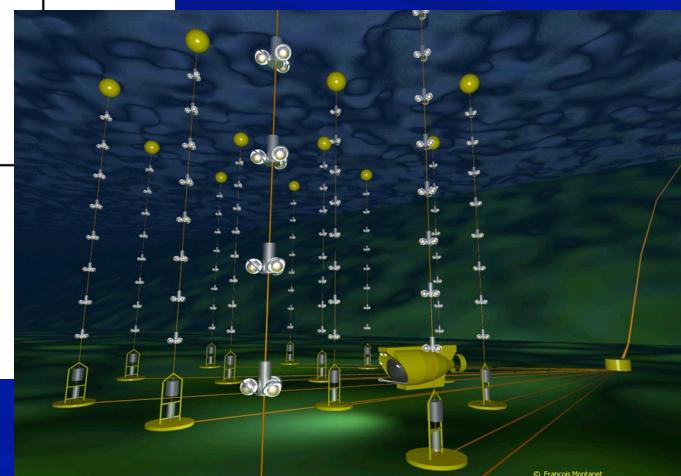
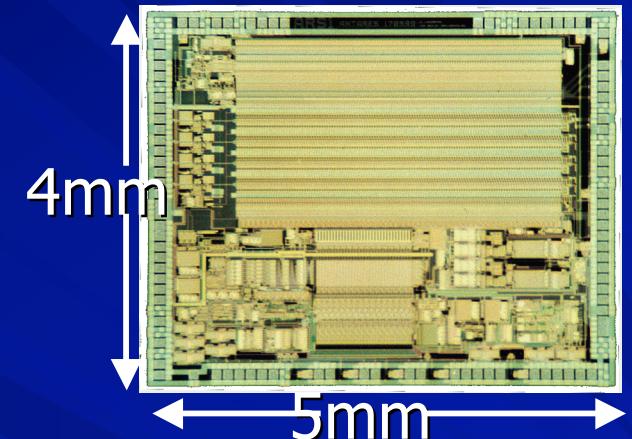
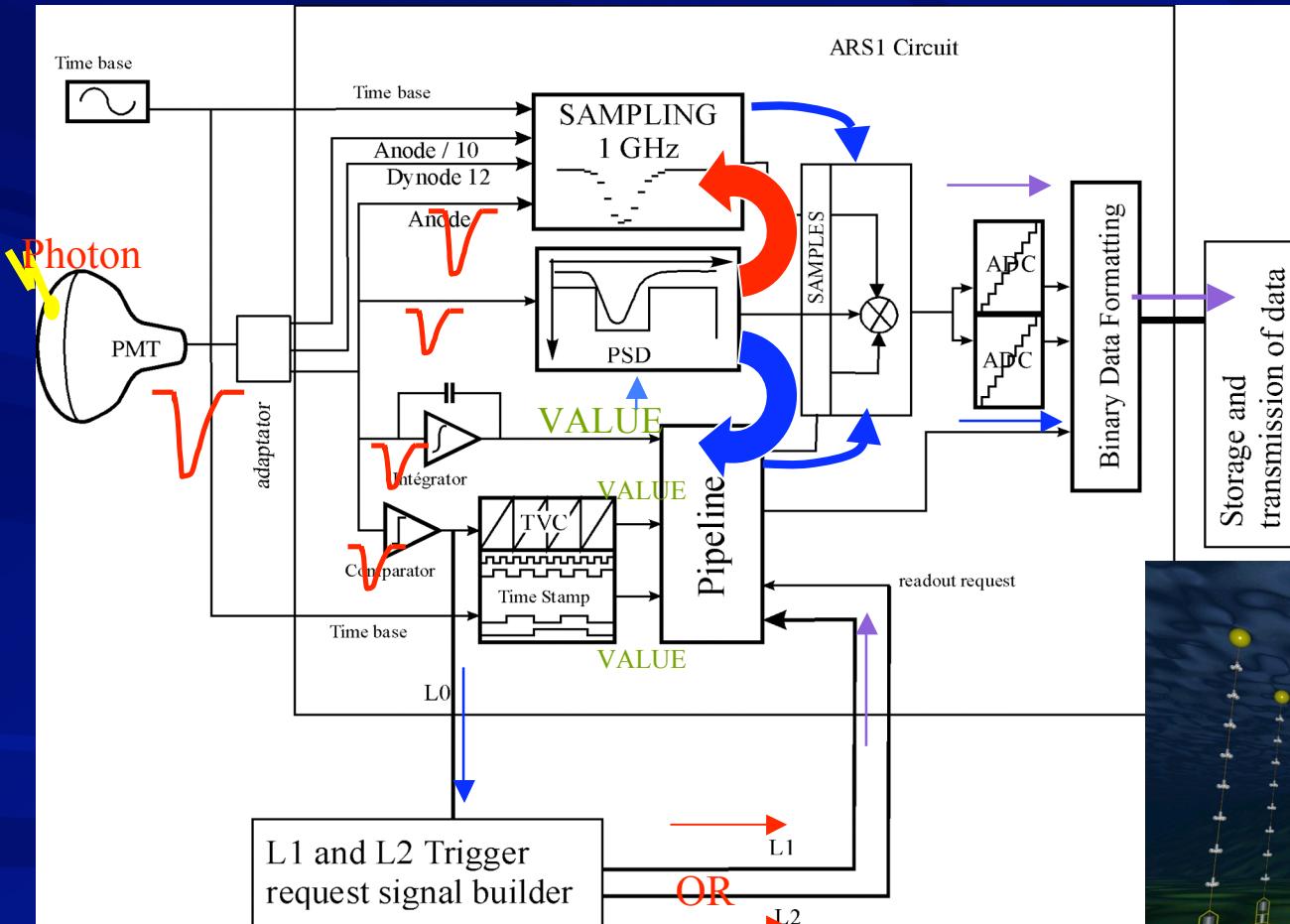
# Towards SoCs...

[E. Delagnes CEA Saclay]



## ■ System On Chip : several functions integrated

- Ex : Front-end chip for Antarès : pipelines 1GHz, TDC, ADCs...



ARS Chip for the Antares Experiment

# Electromagnetic compatibility (EMC-EMI)

## ■ Coexistence of low and high level signals

- Capacitive coupling, inductive coupling, common impedance coupling
- Still Ohm's law (sometimes Maxwell), but a full lecture...



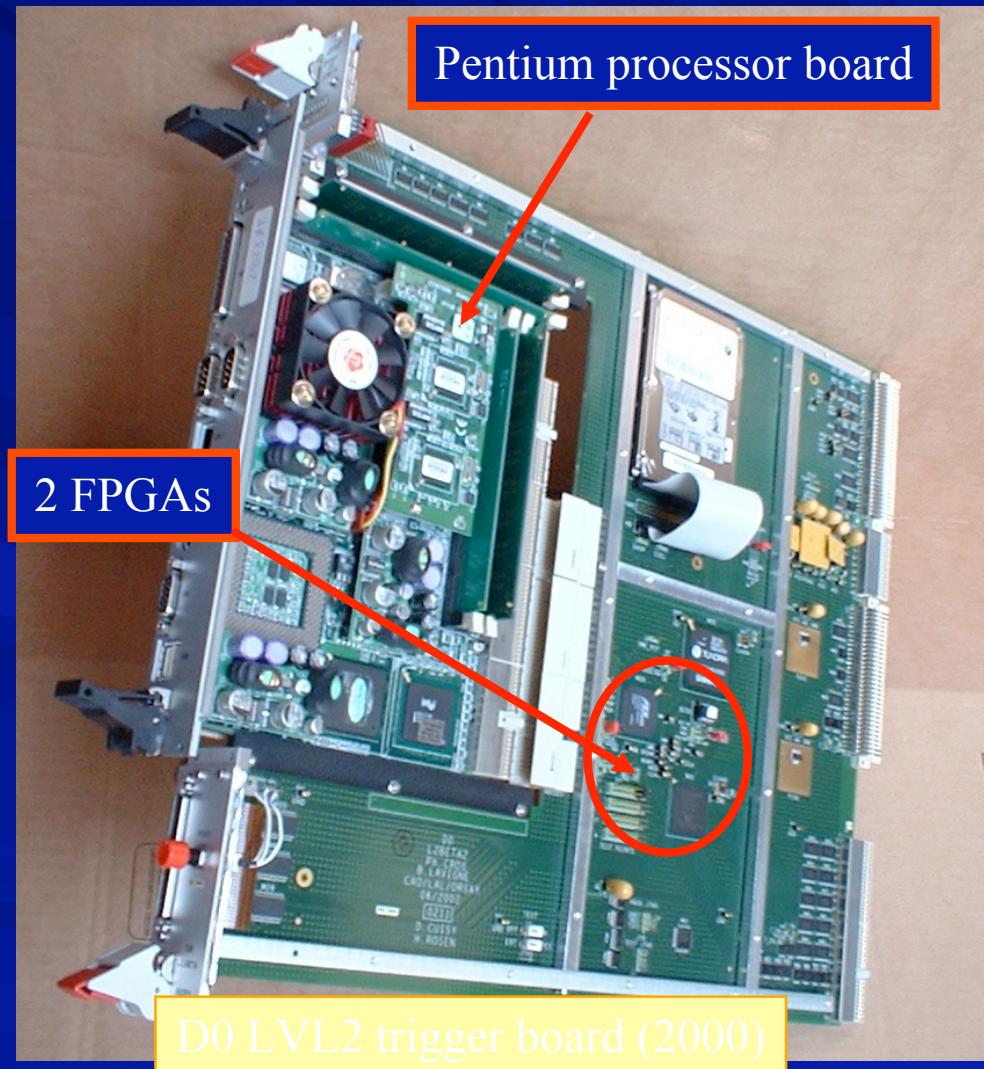
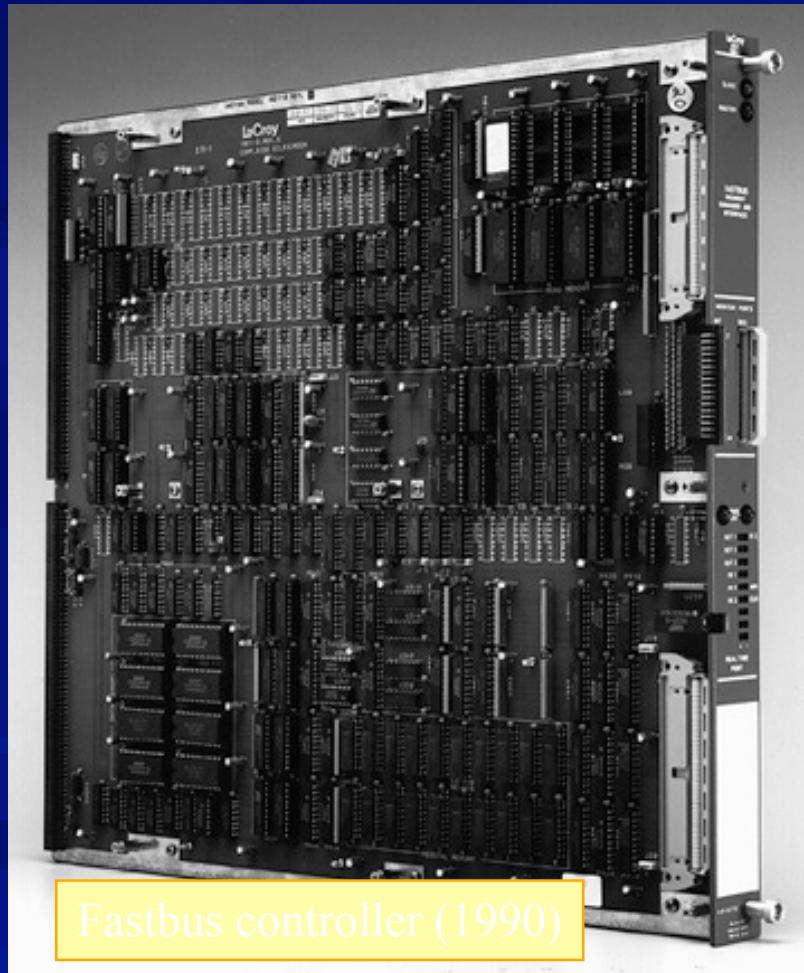
## Radiation hardness : space vs LHC

	<i>Space missions</i>	<i>LHC experiments</i>
■ Mission Time	<i>10-15 years</i>	<i>10 years</i>
■ Service	<i>Not Possible</i>	<i>Impractical</i>
■ Electronics Reliability	<i>High</i>	<i>High</i>
■ Total Dose Requirements	<i>10 -100 krad</i>	<i>1 krad - 10 Mrad</i>
■ Non Ionizing Energy Loss (N)	<i>~0</i>	<i><math>10^{13}</math>-<math>10^{15}</math> N/cm<sup>2</sup></i>
■ Single Event Upsets	<i>IC's SEU characterised</i> <i>No Critical SEU Accepted</i>	
■		



# Evolution of digital electronics (1)

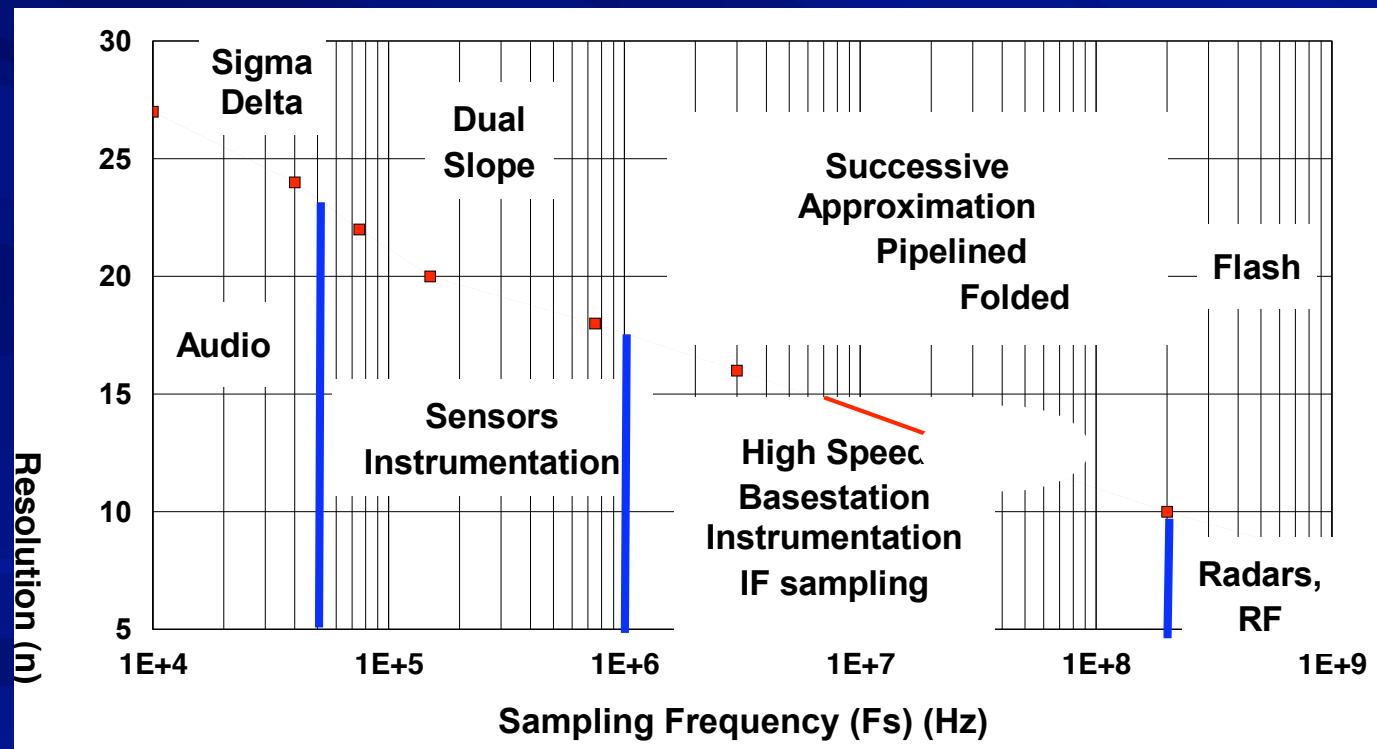
- From arrays of circuits to FPGAs : programmable logic



# ADCs : G.D.A.S.A.P.

[L. Dugoujon LEB8 Colmar 02]

- Thrust to G.D.A.S.A.P. : « go digital as soon as possible »
  - Spectacular evolution of ADCs : more bits, faster (2002 : 14 bits 65 MHz)
  - Power reduction : 12 bits 40 MHz @ 250 mW
  - Propelled by evolution of technologies and telecom



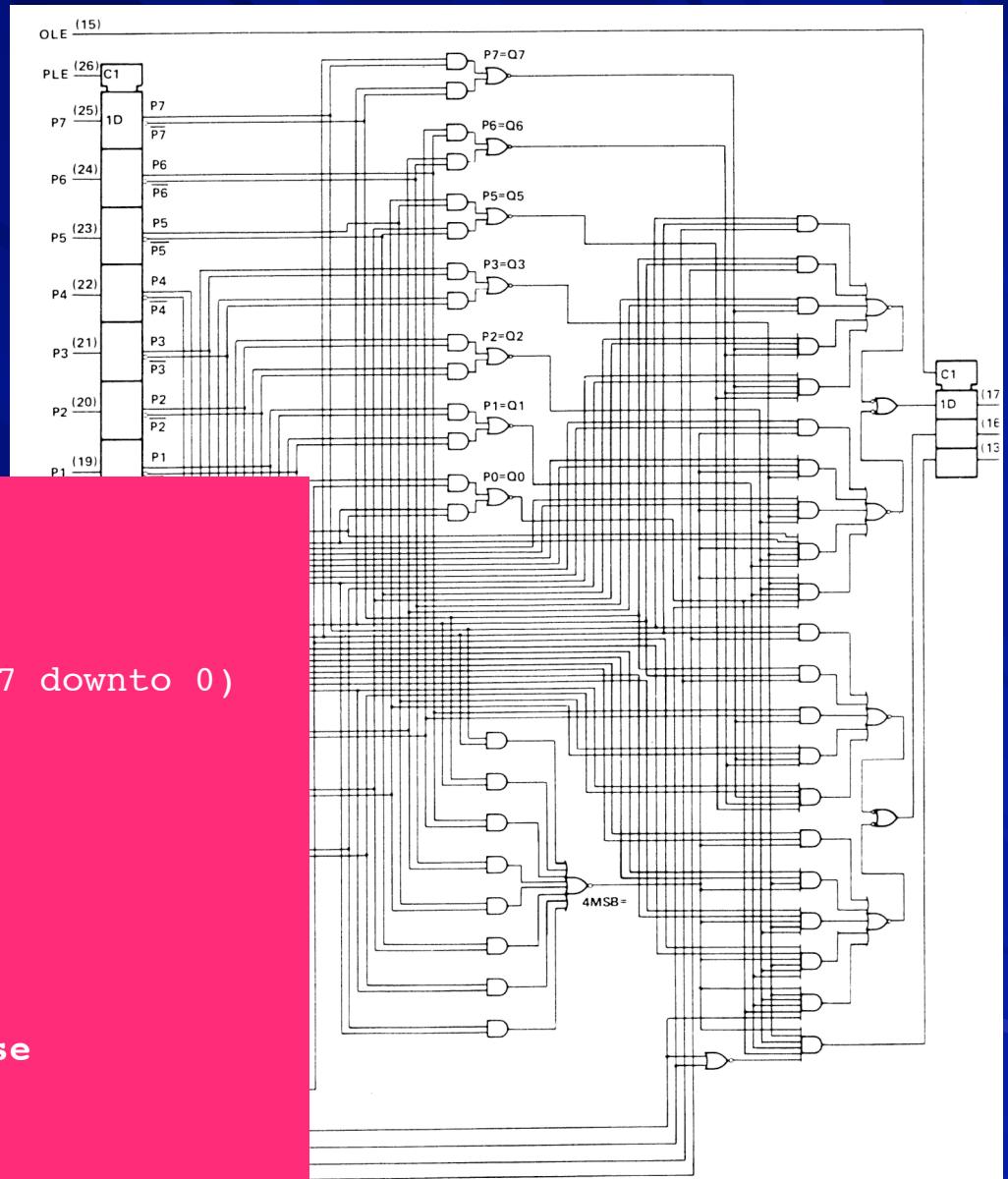
Resolution vs speed of ADCs in 2002

# Evolution of digital electronics (2)

- Schematic -> High level
- Languages (**Verilog, VHDL**)
  - Example 8 bit comparator
  - 74LS866

## VHDL comparator :

```
entity comparator_8 is
port (  raz : in std_logic;
        val1,val2 : in std_logic_vector(7 downto 0)
        result : out std_logic
      );
end entity comparator_8;
architecure archi_& of comparator_8 is
begin
  result <=  '0' when raz = '0' else
            '1' when val1 > val2 else
            '0'
end architecture archi_1;
```



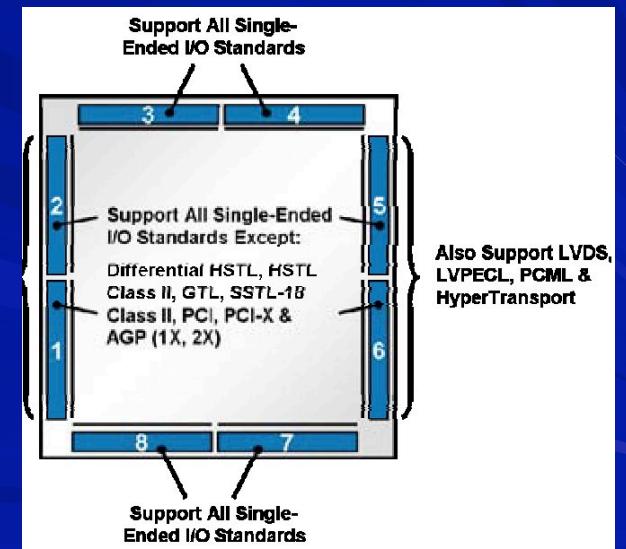
# Evolution of digital electronics (3)

## ■ Reduction of digital logic levels

- 1980 : TTL : 0-5 V
- 2000 : LVDS : Low Voltage ( $\pm 400$  mV) Differential Swing
- Better signal integrity (EMC)
- Reduction of power supplies 5V  $\rightarrow$  3.3V  $\rightarrow$  2.5V  $\rightarrow$  1.2V

## ■ Components : the revolution of FPGAs :

- = Field Programmable Arrays (Altera<sup>©</sup>, Xilinx<sup>©</sup>)
- 4-40 millions gates (55M in a Pentium4)
- RISC 32bits processors
- 10 Mbits resident memory
- 2000 pins 1300 I/O (inputs/outputs)
- 300 MHz operation



# FPGAs as blackhole of digital electronics

RISC  
processors

IP standard  
interfaces  
(Ethernet,  
USB,PCI..)

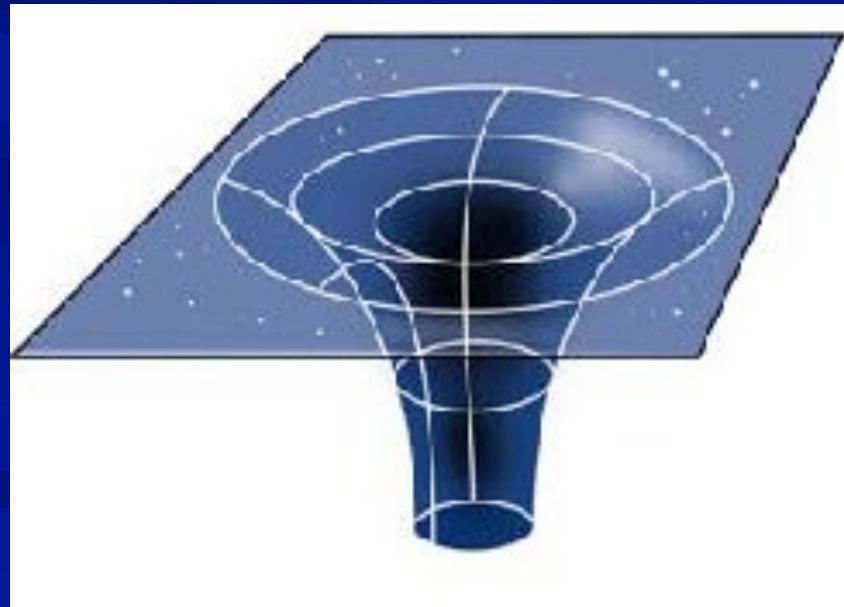
Clocks  
& PLLs

Matching  
networks

DSP blocks,  
arithmetics

Memories  
& FIFOs

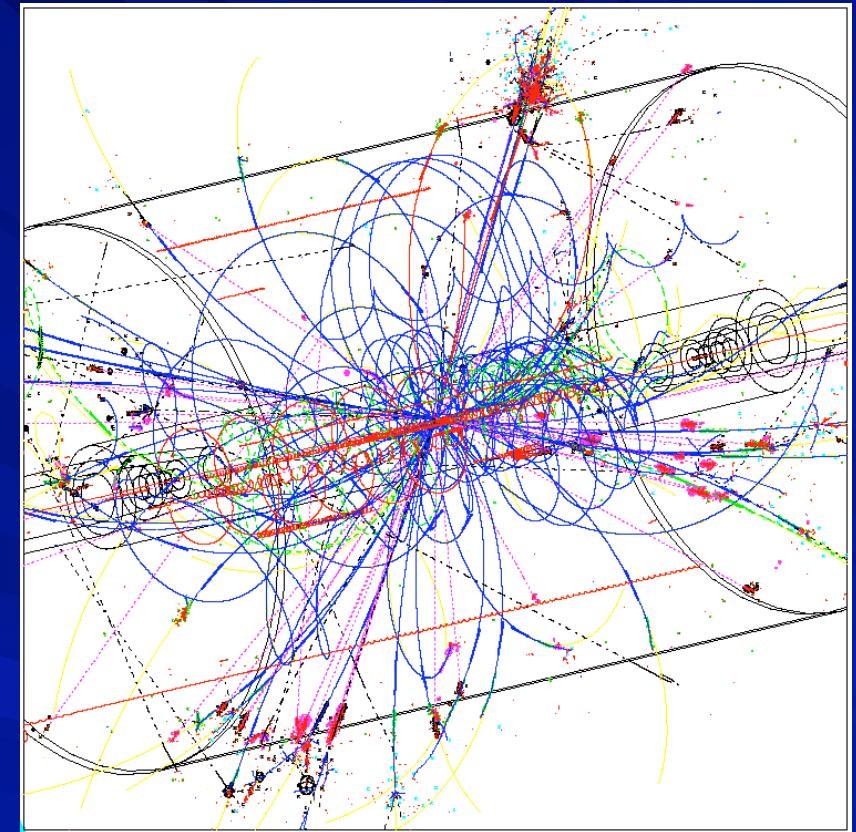
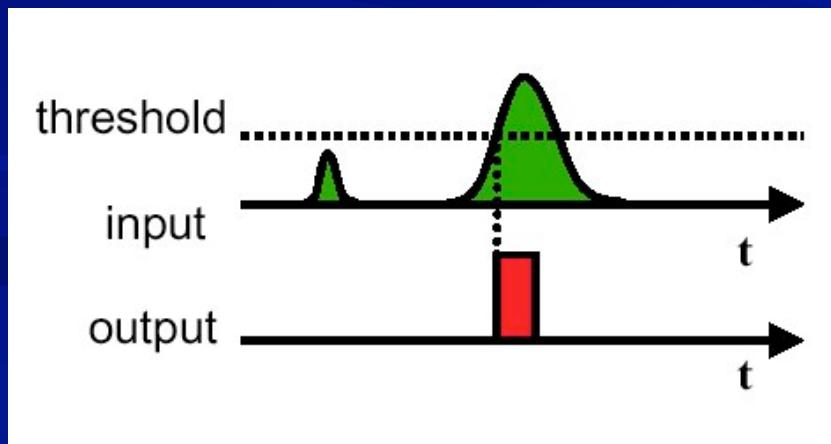
Bus  
interfaces  
(GTL, LVDS...)



# Tracker electronics

## ■ Measuring tracks of charged particles

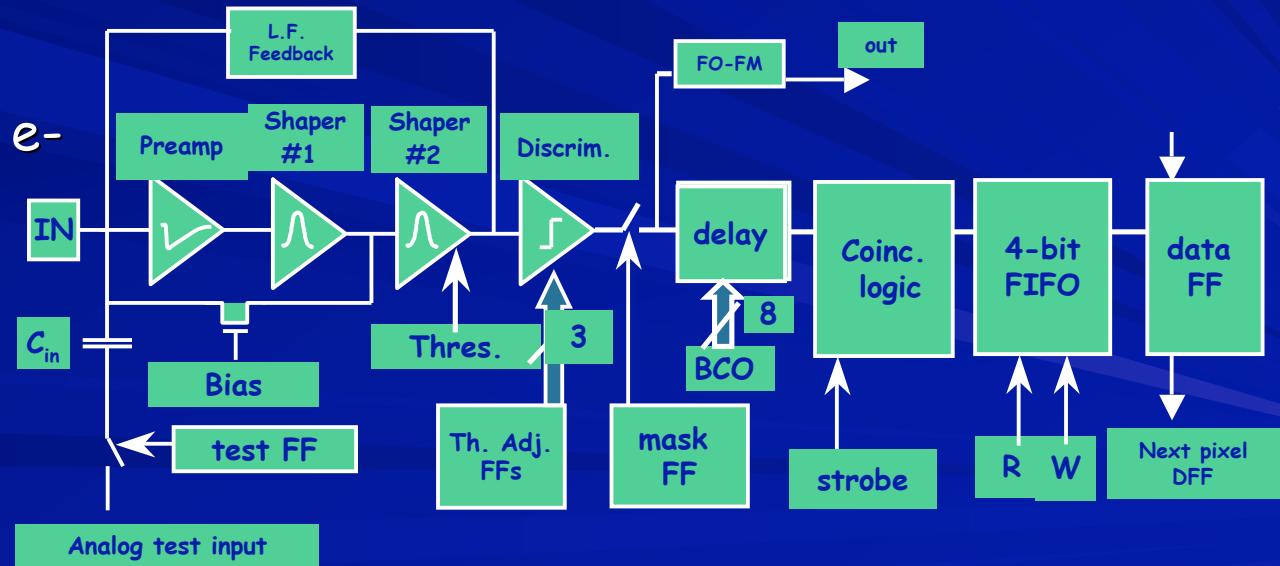
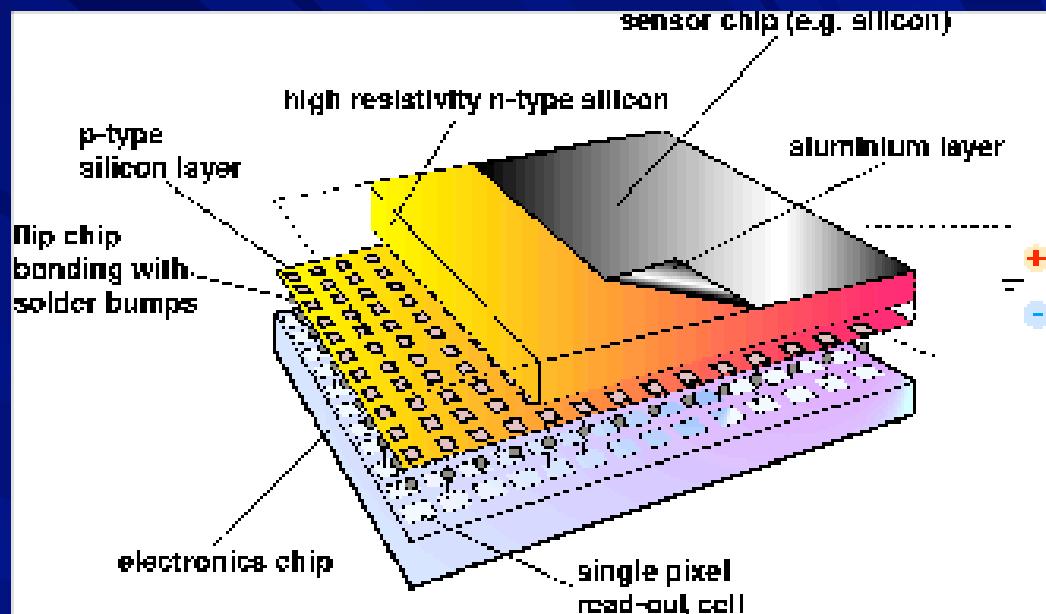
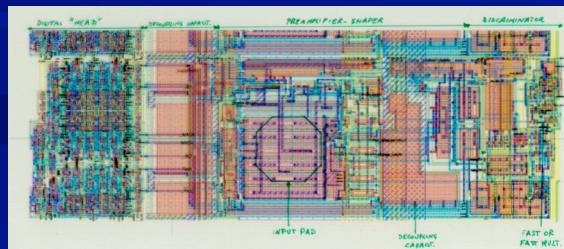
- millions of pixels a few hundred  $\mu\text{m}$
- Very small signals  $\rightarrow$  high amplification
- Binary (or quasi) readout
- Small detector capacitance ( $\sim \text{pF}$ )
- Low power, high speed, low material
- High radiation hardness
- $\Rightarrow$  ideal for ASICs



# Alice-LHCb pixel detector

[P. Jarron]

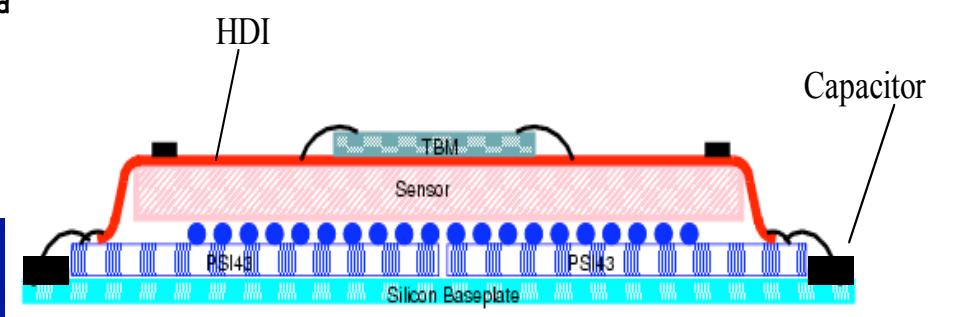
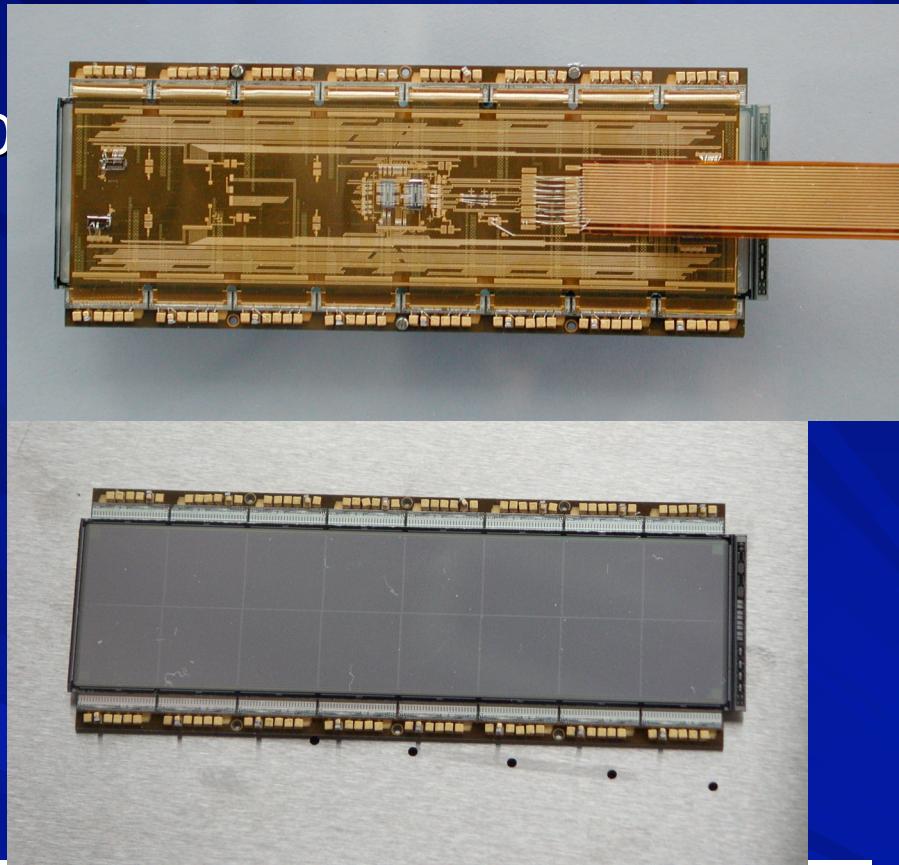
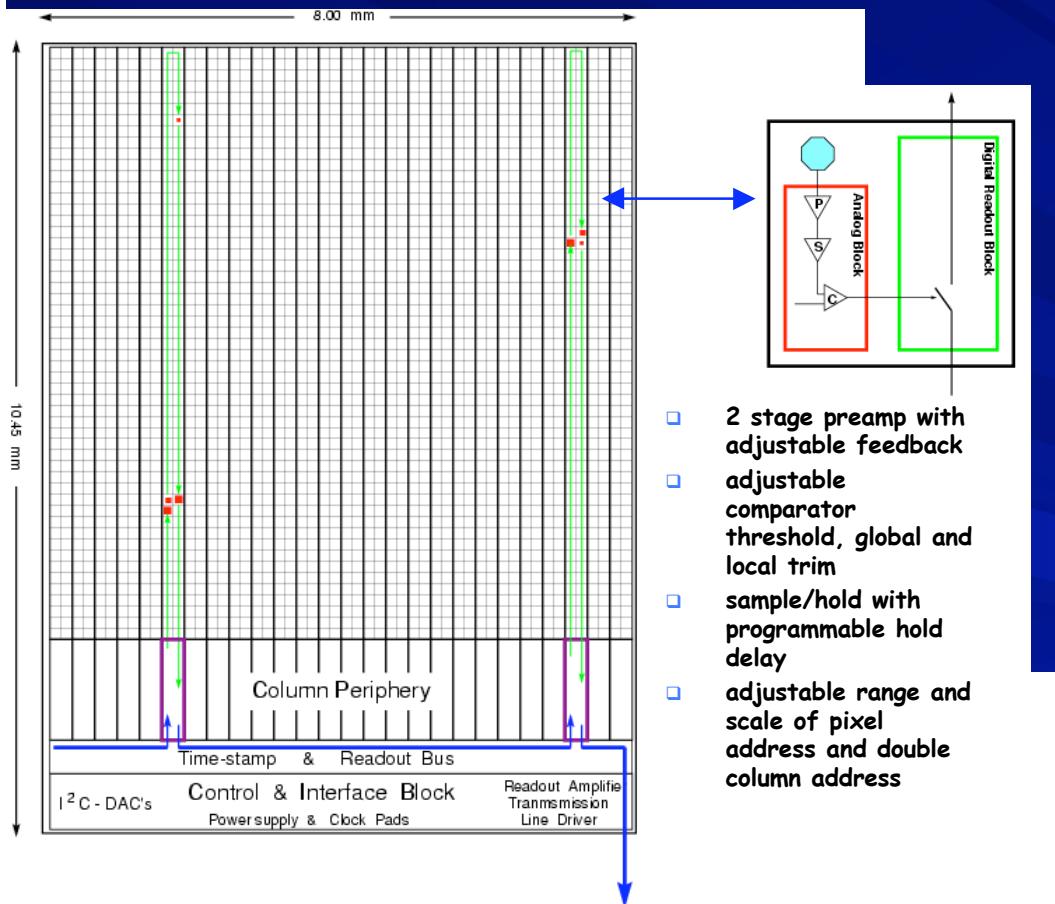
- 8192 pixel cells/die
- 13 millions transistors/die
- 5 dies /detector
- Differential preamp
- Power/die:0.8W
- Pixel size:50 x 450 mm
- All processing functions on pixel
- ENC = 100 e- rms @  $C_{det}=0.1\text{pF}$
- Threshold mismatch:150 e- rms
- Vdd=1.8V

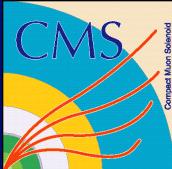


# CMS Pixel...

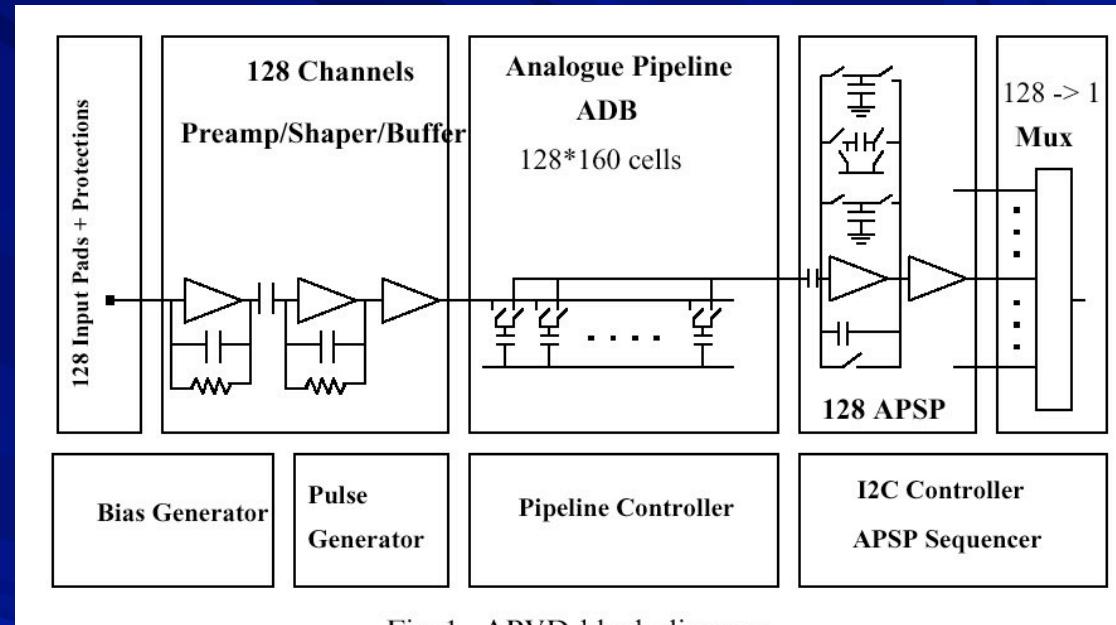
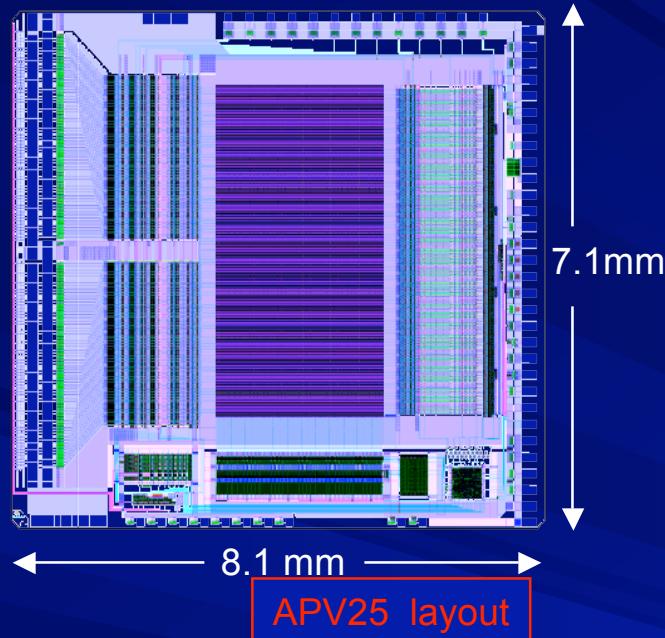


- Ex : pixels trackers
  - Chips of 52x53 pixels of 150x150

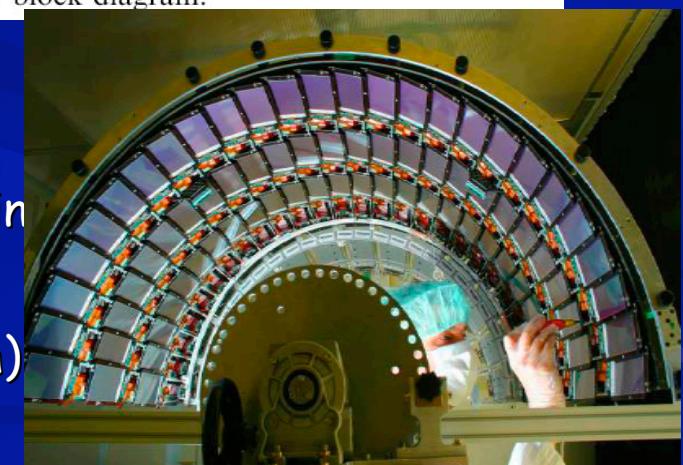




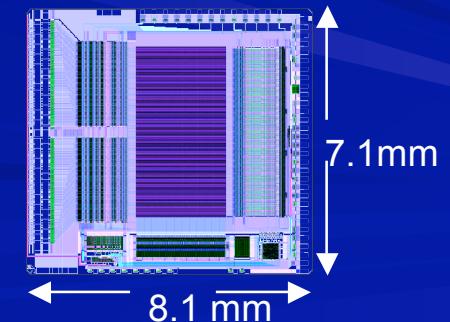
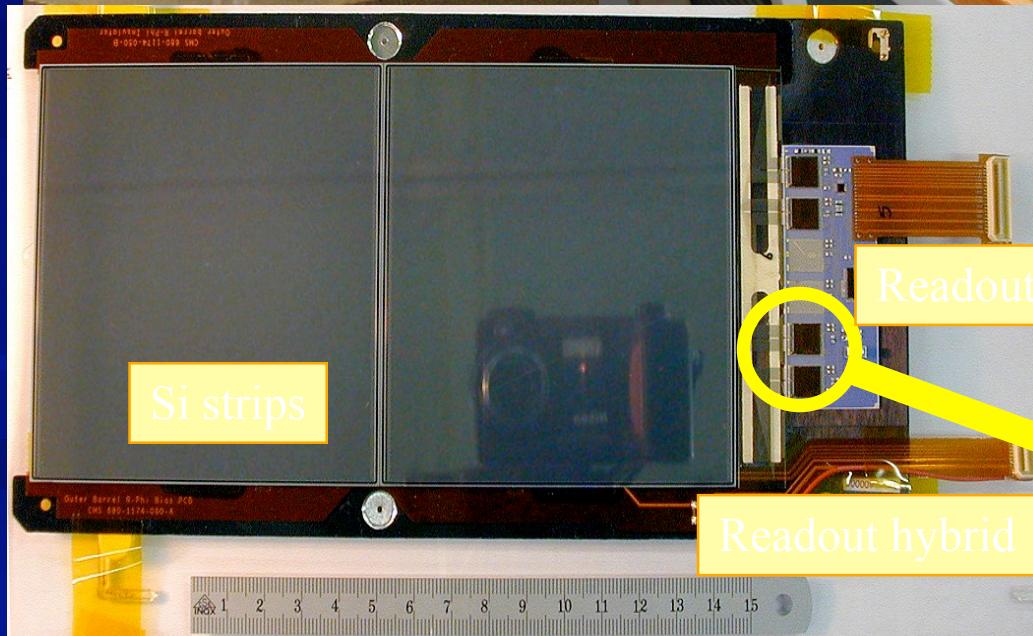
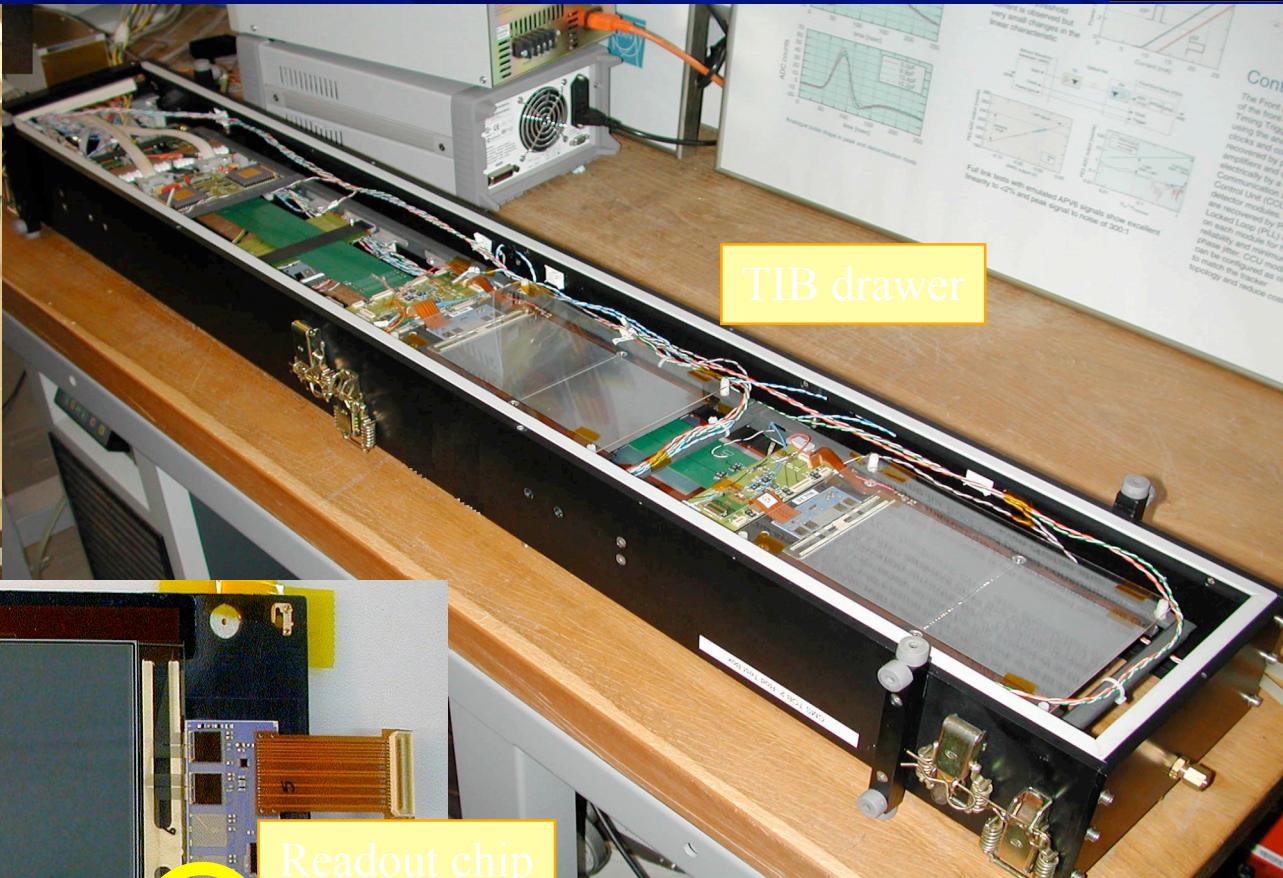
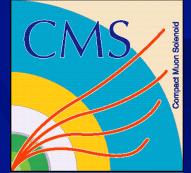
# Trackers circuits : example



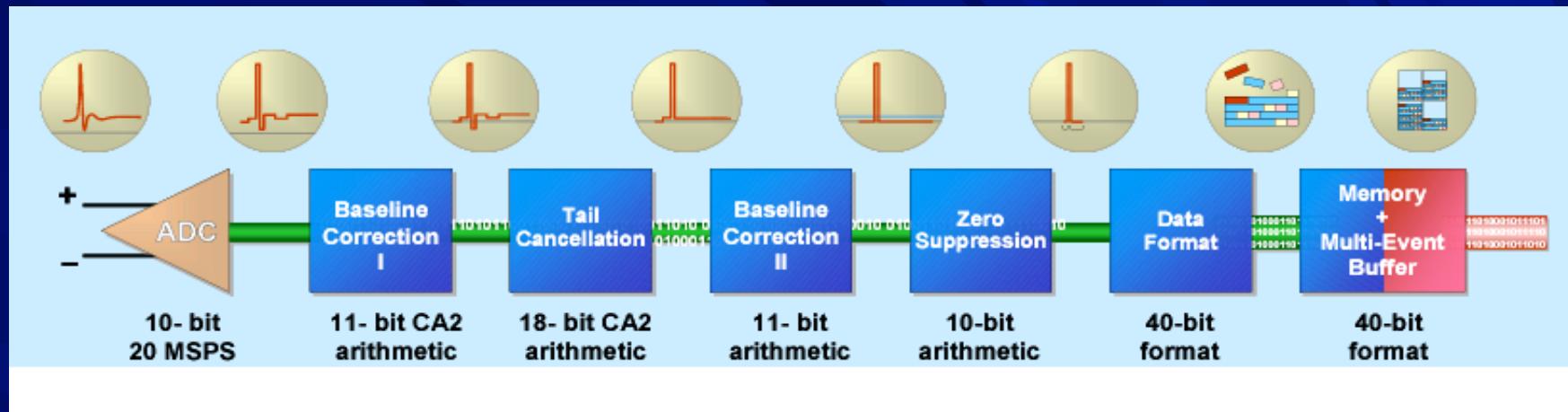
- Very high level of integration
  - 128 preamps/shapers, 128\*160 analog pipelines
  - Mode peak & déconvolution, multiplexe'd output, in
- Performance
  - Dynamic range  $\pm 13$  MIP, low dissipation ( $2\mu\text{W}/\text{ch}$ )
- Rad hard design
  - $0.25\mu$  technology, withstands 50 Mrads



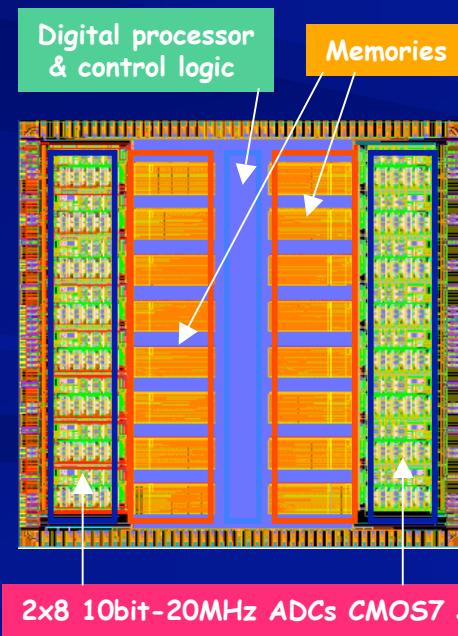
# Tracker electronics



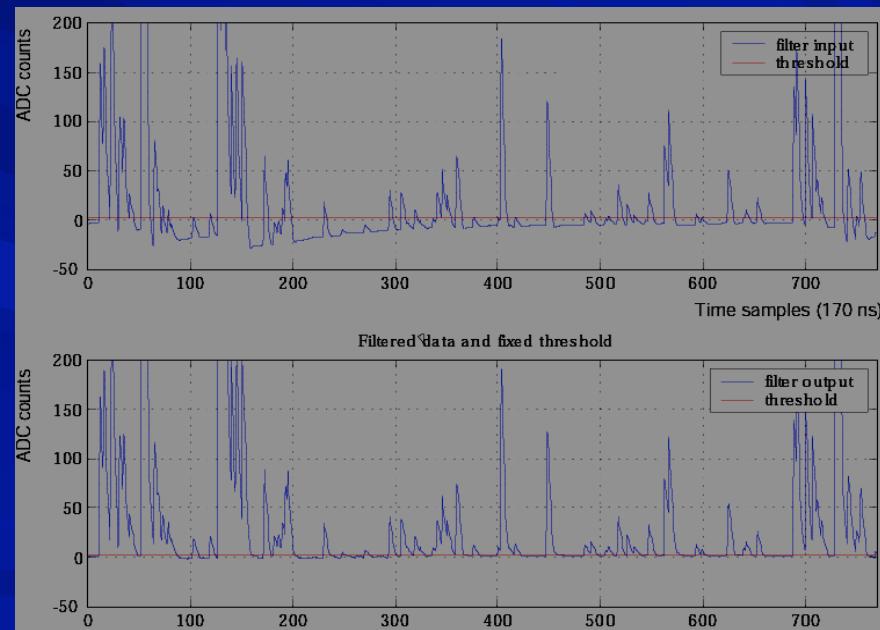
# ALTRO chip ALICE TPC



- 8-ch ALTRO readout chip  
-64 mm<sup>2</sup>, 29mW/ch



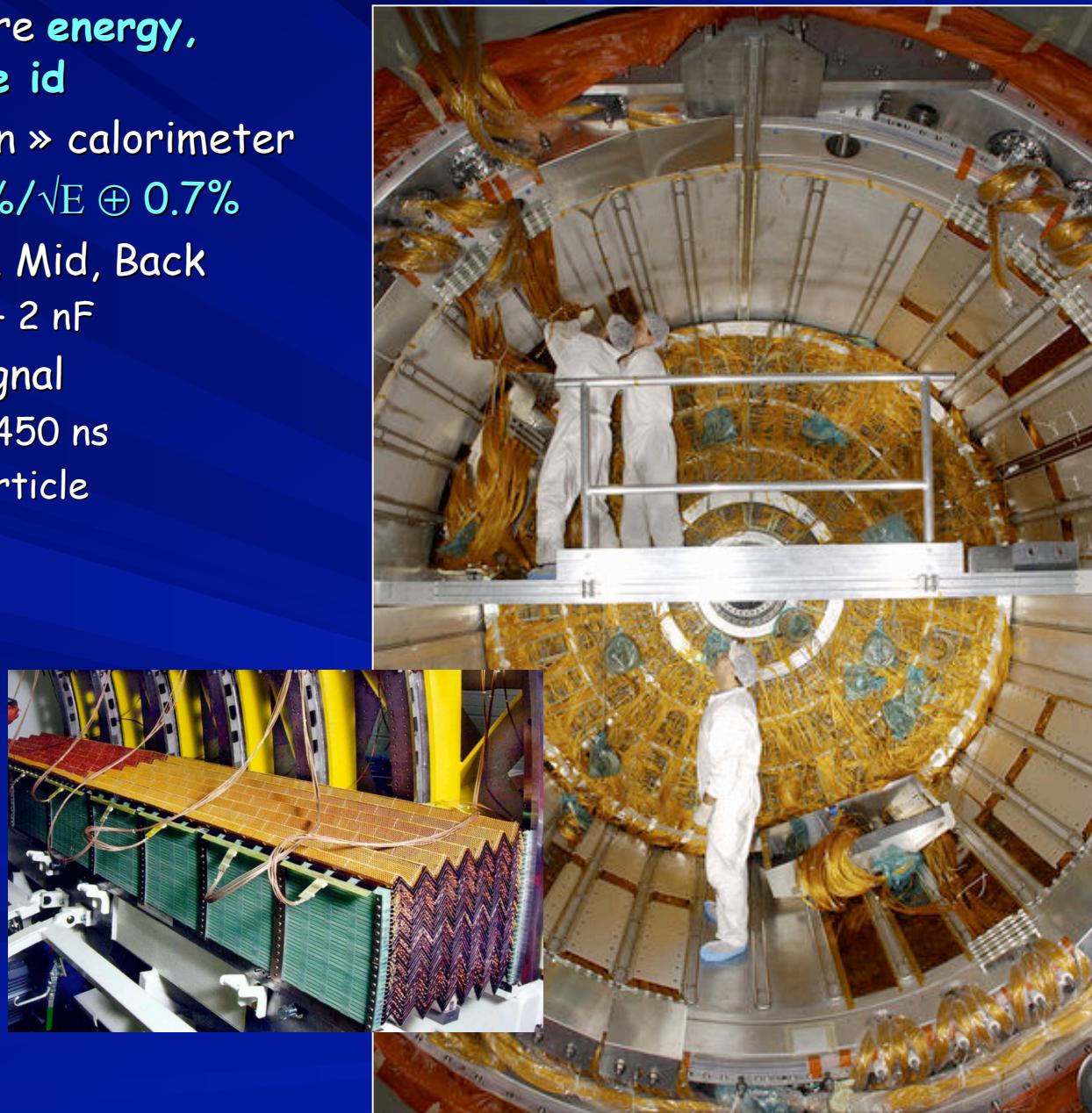
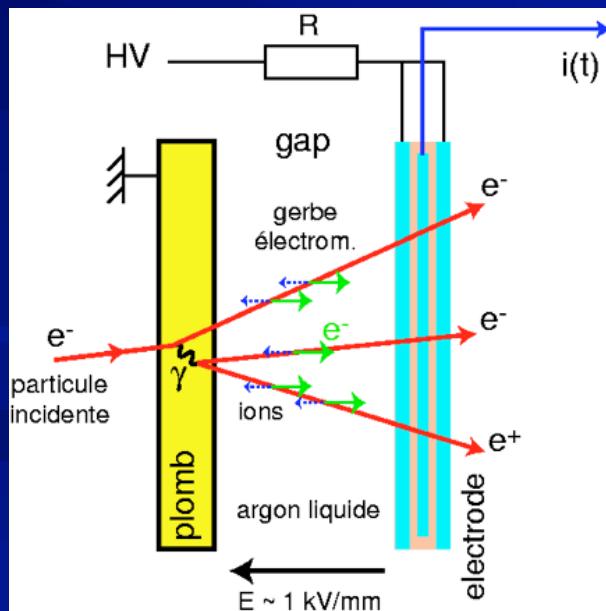
After L. Musa/CERN





# ATLAS : LAr e.m. calorimeter

- Ex calorimetry : measure **energy, position, time, particle id**
- Liquid argon « accordion » calorimeter
- Energy resolution :  $10\%/\sqrt{E} \oplus 0.7\%$
- Segmentation : PS, Frt, Mid, Back
  - Capacitance :  $200 \text{ pF} - 2 \text{ nF}$
- Triangular ionisation signal
  - $I_0 = 2.5 \mu\text{A}/\text{GeV}$   $t_{dr} = 450 \text{ ns}$
  - $I_0$  proportionnal to particle

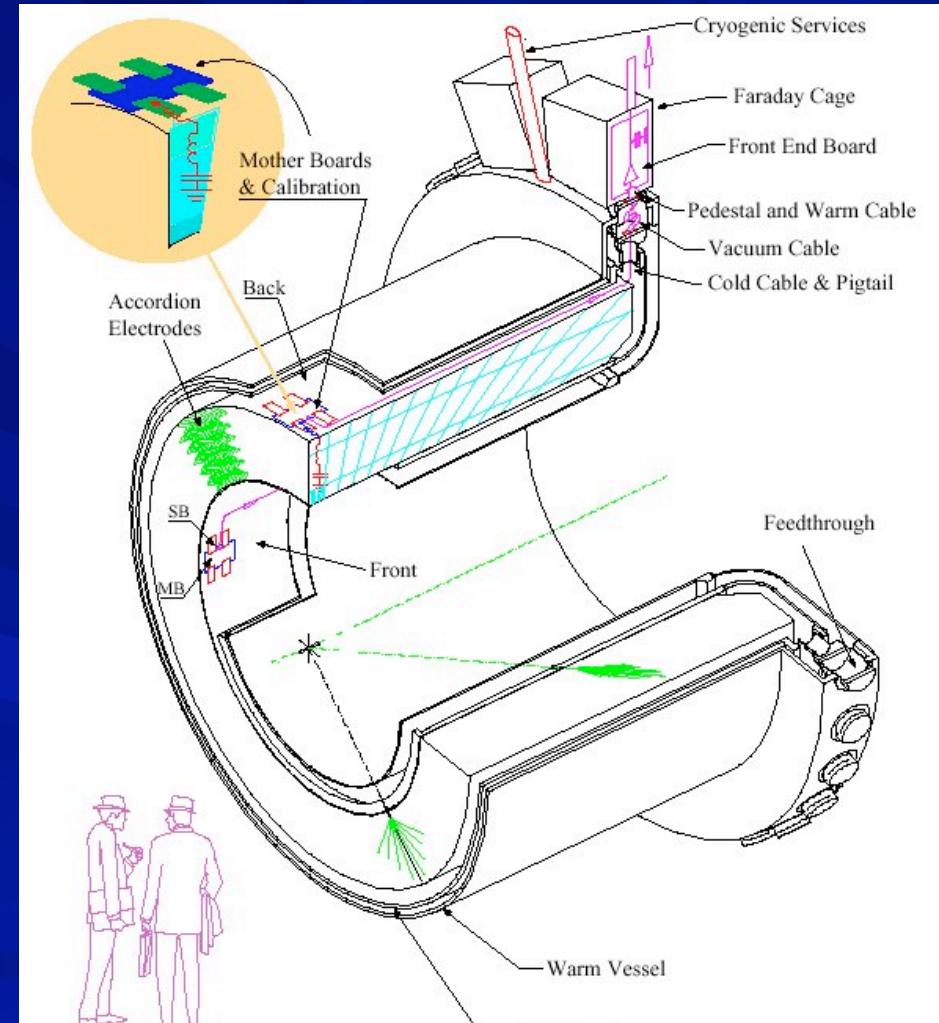




# Calorimeter electronics

## ■ Measuring the energy of particles

- Large dynamic range : 16 bits (**50 MeV-3 TeV**)
- High accuracy ( $\sim\%$ ) and linearity ( $\%$ )
- Low noise, high speed
- Large Capacitance : 200 pF - 2 nF
- 200 000 channels, more power
- Radiation tolerance required



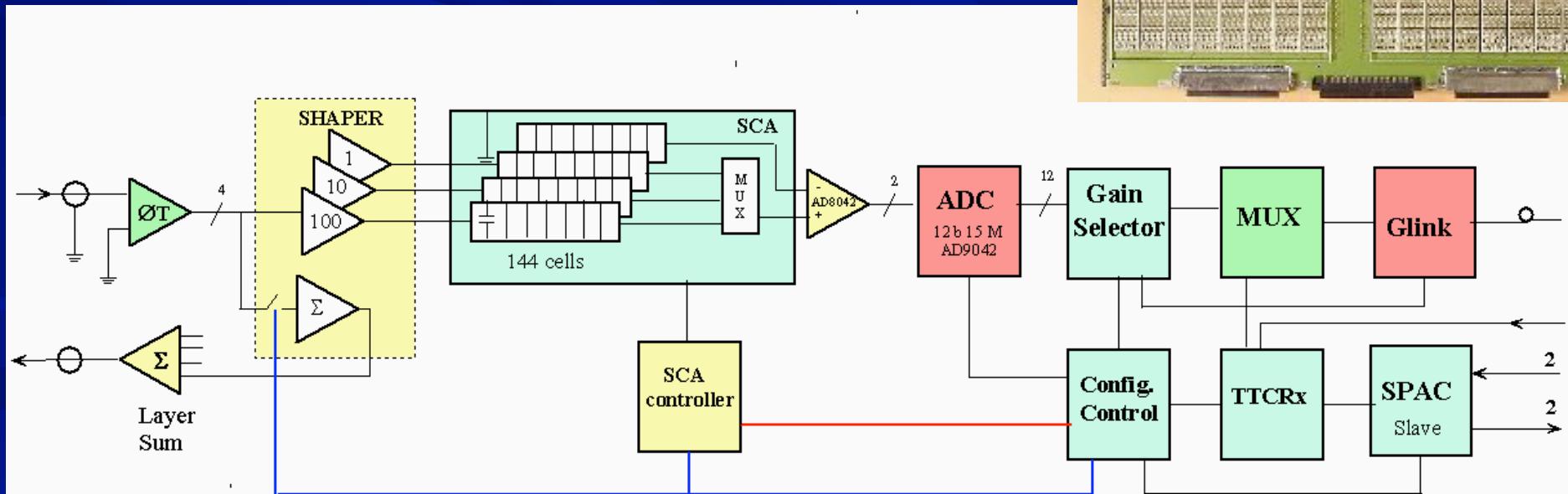
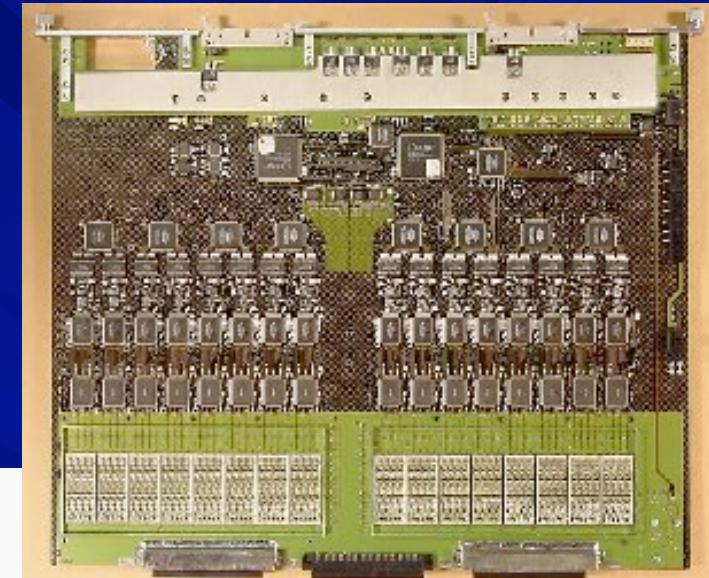
ATLAS LAr calorimeter



# ATLAS LAr : Front End boards

- Amplify, shape, store and digitize Lar signals

- 16 bits dynamic range current preamps
- Trigain (1-10-100) CRRC<sup>2</sup> shapers
- 12 bits R/W analog memories
- 10 different ASICs rad hard...



# Conclusions

- A real move towards smart sensors
- micro-electronics getting closer to detector Unavoidable with increase of channels number
- Cost reduction
- Backend more and more integrated Integration of ADC Signal processing
- Loading of parameters

